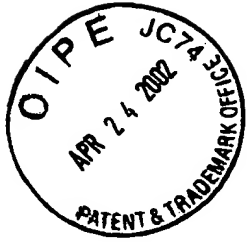


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
"INFORMATION DISCLOSURE STATEMENT"



APPLICANT: Stanley A. WHITE

Honeywell Docket No.
H0002453US

ATTY DOC. NO. P02,0154

SERIAL NO: 10/928,512

GROUP ART: Unknown

DATE FILED: August 13, 2001

EXAMINER: Not Yet Assigned

INVENTION: "HARMONIC SERIES FILTER"

Assistant Commissioner for Patents
Washington D.C. 20231

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SIR:

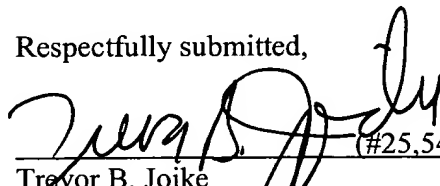
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The patents and/or publications listed on the enclosed PTO 1449 form are submitted pursuant to 37 CFR §§ 1.56, 1.97, and 1.98. Copies of the patents and/or publications noted on the PTO1449 form are enclosed herewith.

This Information Disclosure Statement is being filed, to the best of the undersigned's knowledge, before the mailing date of a first Office Action on the merits. Therefore, in accordance with 37 CFR §1.197(b), no certification or fee is required.

An early and favorable action on the merits is respectfully requested.

Respectfully submitted,


(#25,542)

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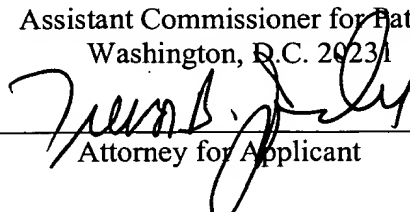
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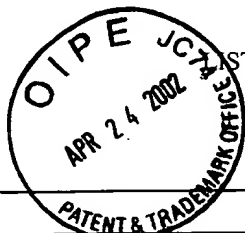
April 19, 2002



Attorney for Applicant

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Form 1449

U.S. Department of Commerce
Patent and Trademark OfficeDocket No.
**Honeywell-
H0002453US**Serial No.
10/928,512LIST OF PRIOR ART CITED BY APPLICANT
(use several sheets if necessary)Applicant(s):
STANLEY A. WHITEFiling Date
August 13, 2001

Group Art Unit

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If appropriate
	AA	5,675,498	OCT. 7, 1997	White			
	AB	5,577,073	NOV. 19, 1996	White			
	AC	5,444,639	AUG. 22, 1995	White			
	AD	5,587,910	DEC. 24, 1996	Woodard			
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	AF						
	AG						
	AH						
	AI						

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FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ							
	AK							
	AL							
	AM							
	AN							
	AO							
	AP							

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OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AQ	A.H. Gray, Jr. & J.D. Markel, "DIGITAL LATTICE AND LADDER FILTER SYNTHESIS"; IEEE Transactions on Audio & Electro-Acoustics, Vol. AU 21, No. 6, December (1973), pgs. 491-500.
	AR	P. A. REGALIA, et al.; "THE DIGITAL ALL-PASS FILTER: A VERSATILE SIGNAL PROCESSING BUILDING BLOCK"; Proceedings of the IEEE, Vol. 76, No. 1, January (1988), pgs. 19-37.
	AS	R. E. BEST, "PHASE-LOCKED LOOPS", Design, Simulation, & Applications, Fourth Edition, Chapter 5, McGraw Hill, pgs. 229-249.
	AT	
	AU	
	AV	
	AW	

Examiner

Date Considered

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.